```
DERWENT-ACC-NO:          [illegible]

DERWENT-WEEK:            [illegible]

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TITLE:                     [illegible]
[illegible]
                         [illegible]
[illegible]
                         [illegible]
[illegible]
                         [illegible]

INVENTOR: MAEYAMA, [illegible]

PATENT-ASSIGNEE:  [illegible]

PRIORITY-DATA: [illegible]

PATENT-FAMILY:
PUB-NO                   PUB-DATE
LANGUAGE        PAGES      MAIN-IPC
EP [illegible] A2             [illegible]                      E
        [illegible]        H01L [illegible]
[illegible] A                 [illegible]                      N/A
        [illegible]        H01L [illegible]
[illegible] A                 [illegible]                      N/A
        [illegible]        H01L [illegible]
[illegible] A                 [illegible]                      N/A
                           H01L [illegible]
KR [illegible] A              [illegible]                      N/A
        [illegible]        H01L [illegible]
US [illegible] B1             [illegible]                      N/A
        [illegible]        H01L [illegible]
[illegible] A                 [illegible]                      N/A
                           H01L [illegible]


DESIGNATED-STATES: AL AT BE CH CY DE DK ES FI FR GB GR IE
IT LI LT LU LV MC MK
NL PT RO SE SI

APPLICATION-DATA:
PUB-NO                   APPL-DESCRIPTOR            APPL-NO
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APPL-DATE
[illegible] N/A
[illegible] [illegible]
[illegible] N/A
[illegible] [illegible]
[illegible] N/A
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[illegible] [illegible]
[illegible] [illegible]
[illegible] N/A
[illegible] March [illegible]
[illegible] [illegible] [illegible]
N/A

INT-CL (IPC): [illegible], [illegible], [illegible],
[illegible],
[illegible], [illegible], [illegible], [illegible],
[illegible],
[illegible], [illegible], [illegible], [illegible],
[illegible]

ABSTRACTED-PUB-NO: [illegible]

BASIC-ABSTRACT:

NOVELTY - A wafer-level package [illegible] includes a
semiconductor wafer [illegible] with
at least one chip forming region [illegible] each including a
semiconductor chip
circuit with test and non-test chip terminals [illegible], at
least one external
connection terminal [illegible], [illegible] [illegible], test
terminal [illegible] and
insulating material. [illegible]
a test chip terminal
and the other [illegible] test terminals [illegible]
portion of the chip
forming region.

DETAILED DESCRIPTION - AN INDEPENDENT CLAIM IS INCLUDED FOR
[illegible]

manufacturing a wafer-level package.

USE - In the manufacture of semiconductor devices.

ADVANTAGE - Improves production efficiency, reduces manufacturing cost,
enables probe test [illegible] to be
implemented on a single
wafer.

DESCRIPTION OF DRAWING(S) - The drawing shows a diagram of
the invention.

Wafer-level package 10A

Semiconductor wafer 11

Chip forming region 12

Test chip terminal 13A

Non-test chip terminals 13B

External connection terminal 14

Redistribution trace 15

Test terminal 16

ABSTRACTED-PUB-NO: US [illegible]

EQUIVALENT-ABSTRACTS:

NOVELTY - A wafer-level package (10A) includes a
semiconductor wafer (11) with
at least one chip forming region (12) each including a
semiconductor chip
circuit with test and non-test chip terminals (13A,13B), at
least one external
connection terminal (14), redistribution trace (15), test
terminal (16) and
insulating material. One end of the trace is connected to
a test chip terminal
and the other end of the test terminals on the outer
region of the chip
forming region.

DETAILED DESCRIPTION - AN INDEPENDENT CLAIM IS INCLUDED FOR:

a method of
manufacturing a wafer-level package.

USE - In the manufacture of semiconductor devices.

ADVANTAGE - Improved manufacturing efficiency, reduced manufacturing cost,
entire process of manufacturing the package can be
implemented on a single
wafer.

DESCRIPTION OF DRAWING(S) - The drawing shows a diagram of the invention.

Wafer-level package 10A

Semiconductor wafer 11

Chip forming region 12

Test chip terminal 13A

Non-test chip terminals 13B

External connection terminal 14

Redistribution trace 15

Test terminal 17

[illegible]

NOVELTY - A wafer-level package (10A) includes a semiconductor wafer (11) with
at least one chip forming region (12) each including a semiconductor chip
circuit with test and non-test chip terminals (13A,13B), at least one external
connection terminal (14), redistribution trace (15), test terminal (17) and
insulating material. One end of the trace is connected to a test chip terminal
and the other end to the test terminals in the outer region of the chip
forming region.

DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is included for a method of

manufacturing a wafer-level package.

USE - In the manufacture of semiconductor devices.

ADVANTAGE - Improves manufacturing efficiency, reduces
manufacturing cost,
[illegible]
implemented [illegible]
wafer.

DESCRIPTION OF DRAWING(S) - The drawing shows a diagram of
the invention.

Wafer-level package 10A

Semiconductor wafer 11

Chip formation region 12

Test chip terminal 13A

Non-test chip terminals 13B

External connection terminal 14

Redistribution trace 15

Test terminal 16

CHOSEN-DRAWING: Dwg.1/12

TITLE-TERMS: WAFER LEVEL PACKAGE SEMICONDUCTOR WAFER CHIP FORMING
REGION TEST NON
TEST CHIP TERMINAL REDISTRIBUTE TRACE WAFER
NON TEST CHIP TERMINAL
EXTERNAL CONNECT TEST TERMINAL

DERWENT-CLASS: U11

EPI-CODES: U11-E02; U11-F02;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2003-[illegible]

L Number	Hits	Search Text	DB	Time stamp
1	[illegible]	wafer with (metal pattern)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
[illegible]	[illegible]	(test testing tester) with (chip die) [illegible] (integrated adj circuit) [illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
[illegible]	[illegible]	(pad terminal electrode) [illegible] with (free wiring)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
4	[illegible]	(wafer with (metal pattern)) and ((test testing tester) with (chip die) [illegible] (integrated adj circuit) [illegible]) and ((pad terminal electrode) [illegible] with (free wiring))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
[illegible]	[illegible]	[illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
[illegible]	[illegible]	(test testing tester) [illegible] with [illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
[illegible]	[illegible]	[illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
[illegible]	[illegible]	[illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
[illegible]	[illegible]	[illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
[illegible]	[illegible]	[illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
[illegible]	[illegible]	[illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]

Double Patenting

3. In claim 1 of the instant application the word " semiconductor " on line 2 is added to the claim. However, the IC die (i.e. integrated circuit die) of U.S. Patent 6,316,824 is a semiconductor die. In claim 1 of the instant application the phrase " at least one bond pad thereon " on line 2 was replaced with " a plurality of bond pads thereon " in U.S. Patent No. 6,316,824. However, at least one bond pad is present in a plurality of bond pads. In claim 1, of the instant application the phrase **for attachment in one of a conventional die attach to lead frame connect process and a LOC connect process is** added to the claim. However, a connector (i.e. bonding wire) is an attachment means for a conventional die to a lead frame. In claim 3, of the instant application the word " semiconductor " on line 2 is added to the claim. However, the IC die (i.e. integrated circuit die) of U.S. Patent 6,316,824 is a semiconductor die. In claim 3 of the instant application the phrase " at least one bond pad thereon " on line 2 was replaced with " a plurality of bond pads thereon " in U.S. Patent No. 6,316,824. However, at least one bond pad is present in a plurality of bond pads. In claim 3, of the instant application the phrase **for attachment in one of a conventional die attach to lead frame connect process and a LOC connect process is** added to the claim. However, a connector (i.e. bonding wire) is an attachment means for a conventional die to a lead frame. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101, which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

4. Claims 1 and 3 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1 and 3 of prior U.S. Patent No. 6,316,824. This is a double patenting rejection.

Double Patenting

4. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101, which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

5. Claims 1-20 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1 and 18 of prior U.S. Patent No. 6,507,109. This is a double patenting rejection.